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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,521	07/13/2001	Satoshi Nakamura	325772024100	2646

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	9

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,521	NAKAMURA, SATOSHI	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *7-17,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 7 –17 and 21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Claim 22 is also withdrawn from further consideration in that it is not deemed to be included in Species I (Fig. 7) for the reason set forth below.

Evidence that claim 22 fails to correspond in scope with that which applicant(s) regard as the elected invention of species I corresponding to Fig. 7, filed 12/4/2003. In the response to election of species requirement, applicant has stated that the species I (Fig. 7) is covered by claims 1-6, 19-20 and 22. However, the invention of species I as described in the specification is different from what is defined in the claim 22. The disclosure of Fig. 7 does not include enablement for the limitation "wherein said second signal processing circuit includes a logarithmic/linear conversion circuit, and wherein said first signal processing circuit receives the second signal processed by the second signal processing circuit." This feature appears to belong to the other species corresponding to Fig. 9 rather than the species corresponding to Fig. 7, or above "said first signal processing circuit" was mistakenly written to mean "said third signal processing circuit" since "said first signal processing circuit" can only join "the second signal processed by the second signal processing circuit" but cannot receive such the second signal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 18 – 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Morris et al (2003/0164884 A1).

Regarding claim 1, Morris discloses a solid-state image sensing apparatus, comprising: a solid-state image sensing device (140) outputting an electrical signal proportional to an intensity of incident light, the solid-state image sensing device configured for outputting a first signal converted linearly to the intensity of the incident light and a second signal converted natural-logarithmically to the intensity of the incident light (see page 2, paragraph [0022]);

a first signal processing circuit (i.e., a portion of circuit 126) supplied with the first signal from the solid-state sensing apparatus and performing a predetermined signal processing; and a second signal processing circuit (i.e., a second portion of circuit 126) supplied with the second signal from the solid-state image sensing apparatus and performing a predetermined signal processing (see page 3, paragraph [0034]).

Regarding claim 18, Morris discloses a solid-state image sensing device controlled to output a first signal and a second signal linearly and logarithmatically proportional to an intensity of incident light (see Abstract and page 2, paragraph [0022]);

a signal processing circuit receiving the first and second signals, the signal processing circuit processing a first signal and a second signal using first predetermined signal processing and a second predetermined signal processing, respectively (see page 3, paragraph [0034]).

Regarding claim 19, Morris clearly discloses in paragraph [0034] that signal processing circuit further comprising: a first signal processing circuit receiving the first signal from the solid-state image sensing device and performing at least a portion of the first predetermined signal processing; and a second signal processing circuit receiving the second signal from the solid-state image sensing device and performing at least a portion of the second predetermined signal processing.

Regarding claim 20, Morris further discloses the signal processing circuit comprising a third signal processing circuit (signal conditioning circuit 148) receiving the first and second signals processed by the first and second signal processing circuits (a first portion and a second portion of signal conditioning circuits 126 including noise filtering), respectively, and performing at least a portion of the first and second predetermined signal processing on the first and second signals (see Fig. 13; page 4, paragraph [0037] and note that the signal processing circuit 148 is coupled to the signal conditioning circuit 126 to perform part of further processing (signal conditioning) of the first and second signals).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4 & 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al (US 2003/0164884 A1) in view of D'Luna et al (US 5,008,739).

Regarding claim 2, Morris discloses the imaging device configured to output a signal in a linear mode or a logarithmic mode, and the output signal in each mode is selected to a first signal processing circuit or a second signal processing circuit, respectively as analyzed in claim 1. Further, Morris also discloses a third signal processing circuit (148) to process signals output from the first and second signal processing circuits as analyzed in claim 20.

Morris fails to explicitly disclose a logarithmic/linear conversion circuit for converting a signal output from the second signal processing (in logarithmic mode) to a signal linearly proportional to the intensity of the incident light before inputting to the third signal processing circuit. D'Luna teaches a log to linear conversion circuit to convert the logarithmic signal to a linear signal for further processing at subsequent states (i.e., black level clamping, interpolation) since the subsequent processes are desirable completed in linear space, where the adjustments

will be direct, linear relation to the charge signal amplitudes existing on the image sensor (see col. 6, lines 1-11).

Therefore, it would have been obvious to one of ordinary skill in the art to include a log to linear conversion circuit on the output of the second signal processing circuit in Morris to convert the logarithmic signal to a linear signal before outputting the signal to the third signal processing for further processing such as black level clamping, interpolation which would require the signal in a linear space, where the adjustments would be direct, linear relation to the charge signal amplitudes existing on the image sensor.

Regarding claim 4, although Morris does not teach that the first processing circuit (for linear characteristics) and the second processing circuit (for logarithmic characteristics) perform gamma correction of the first signal and second signal, respectively, D'Luna suggests an obvious signal processing arrangement wherein the gamma correction can be done in either linear or logarithmic space (see col. 2, lines 18-21).

Therefore, it would have been obvious to enable gamma corrections in both the first and second processing circuits in Morris prior to the third signal processing circuit as an obvious processing variation.

Regarding claim 6, see the analysis in claim 2.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al and D'Luna et al as applied to claim 2 and in further view of Nakamura et al (US 5,289,286).

Regarding claim 3, in the combination of Morris and D'Luna, a multi-color image sensor configured to output color signals in linear mode and logarithmic mode is disclosed (see Title & Fig. 3 in D'Luna and claim 2). Morris and D'Luna do not explicitly disclose white balance adjustment performed in both the processing circuits of linear and logarithmic characteristics. As taught by Nakamura, the white balance has to be established on the output signals to adjust white balance of an output image regardless the output characteristics from an image sensor being linear (conventional) or logarithmic (see col. 2, lines 14-17 and col. 4, lines 28-35).

Therefore, it would have been obvious to one of ordinary skill in the art to further include white balance adjustment in both the first and second processing circuits in Morris and D'Luna to adjust the output signals to an appropriate level when a color temperature of a light source changes.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al and D'Luna et al as applied to claim 2 and in further view of Edwards (US 5,438,360).

Regarding claim 5, the logarithmic mode produces wide dynamic range and is mostly selected for enabling machine vision in the digital camera in Morris (see paragraphs [0022] & [0024]). However, Morris and D'Luna do not teach that a dynamic range of the second signal is adjusted at the second signal processing. Edwards teaches a dynamic range transform logic circuitry (26, 28, 30) being implemented in a machine vision camera to adjust dynamic range of each pixel value by automatically varying the gain for each pixel so as the most useful

information from the extended dynamic of the image is extracted. This reduces the amount of information that must be processed and enables use of an 8-bit A/D converter and also permits real-time processing of the respective image hardware of reduced complexity and cost (see col. 2, lines 59 – col. 3, line 5 & col. 5, lines 14-15).

Therefore, it would have been obvious to one of ordinary skill in the art to implement the second signal processing circuit in the Morris with the dynamic range transform logic circuitry to extract the most useful information from the extended dynamic range of an image by varying the gain for each pixel value since this restriction of dynamic range reduces the amount of information that must be processed and would enable use of an 8-bit A/D converter in signal conditioning circuit 126 of Morris to permit real-time processing of the respective image hardware of reduced complexity and cost.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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